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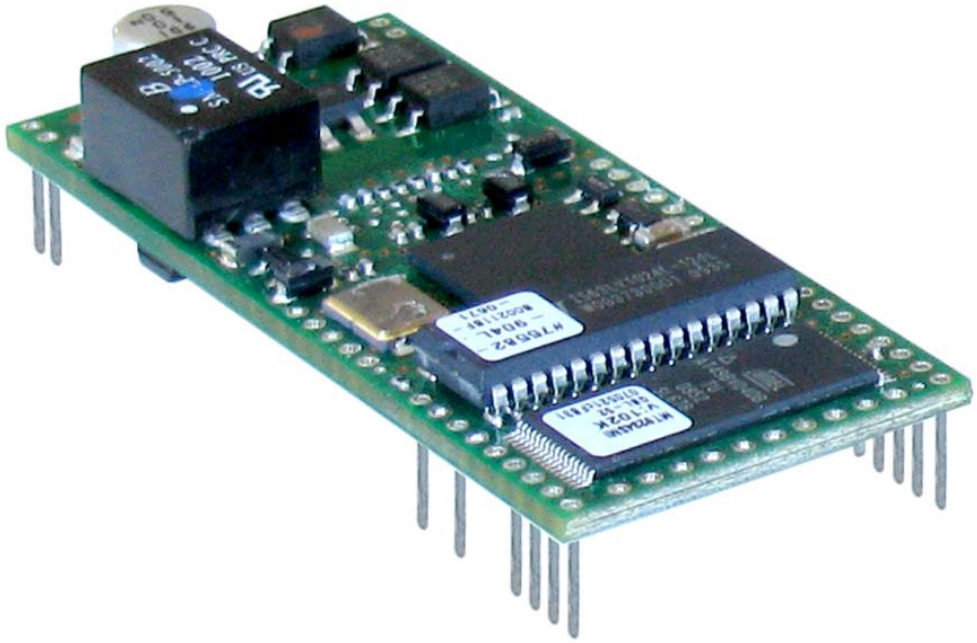

SocketModem®

MT9234SMI Device Guide

SocketModem Device Guide

S000534, Version A

MT9234SMI-92, MT9234SMI-L-92, MT9234SMI-P-92, MT9234SMI-P-L-92, MT9234SMI-HV-92, MT9234SMI-P-HV-92

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Revisions

Revision	Date	Description
A	12/05/12	Initial release. Information was part of the Universal Socket Developer Guide.

Contacting Multi-Tech

Knowledge Base

The Knowledge Base provides immediate access to support information and resolutions for all Multi-Tech products. Visit http://www.multitech.com/kb.go.

Support Portal

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Warranty

To read the warranty statement for your product, please visit: http://www.multitech.com/warranty.go.

Contents

Chapter 1 – Device Overview

Description

The Multi-Tech SocketModem embedded modem creates communication-ready devices by integrating data/fax modem functionality into a single, universal socket design. The SocketModem embedded modem use a space-efficient design that allows OEMs to integrate a wide range of modem functions and speeds into any product platform. The complete, ready-to-integrate modem dramatically reduces development time and costs for system designers. The SocketModem embedded modem complies with telecom requirements globally and can be shipped worldwide.

Product Build Options

Product	Description	Region
MT9234SMI		
MT9234SMI-92	V.92 Serial Data, V.34 Fax, 5V	Global
MT9234SMI-L-92	V.92 Serial Data, V.34 Fax, 3.3V	Global
MT9234SMI-P-92	V.92 Parallel Data, V.34 Fax, 5V	Global
MT9234SMI-P-L-92	V.92 Parallel Data, V.34 Fax, 3.3V	Global
MT9234SMI-HV-92	V.92 Serial Data, V.34 Fax, High Voltage, 5V	Global
MT9234SMI-P-HV-92	V.92 Parallel Data, V.34 Fax, High Voltage, 5V	Global
Telecom Label		
MT9234SMI-LS	MT9234SMI – Global Regulatory Label	Global
Developer Kit		
MTSMI-UDK	Universal Developer Kit	Global
MTSMI-P-UDK	SocketModem Parallel Developer Kit	Global

Notes:

HV indicates High Voltage 2 KV Dielectric Isolation (EN60601)

All builds can be ordered individually or in 50-packs.

The complete product code may end in .Rx. For example, MT9234SMI.Rx, where R is revision and x is the revision number.

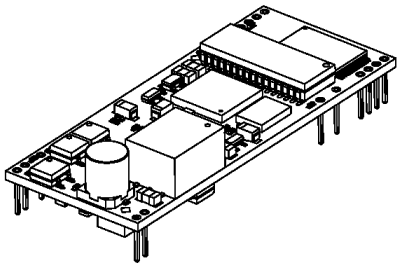
Documentation

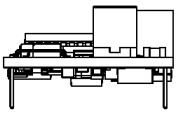
The following documentation is available by email to oemsales@multitech.com or by using the Developer Guide Request Form on the multitech.com website.

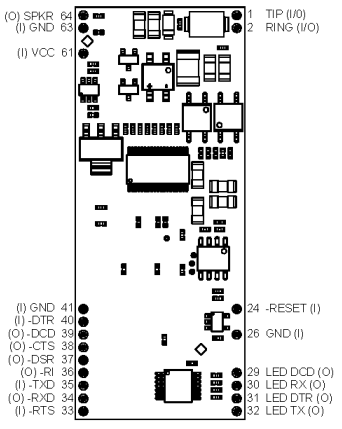
- **Device Guides** – This document. Provides model-specific specifications and developer information.
- **Universal Socket Developer Guide** – Provides an overview, safety and regulatory information, design considerations, schematics, and general device information.
- **AT Command Guide** – Use S000434 the MT9234SMI AT Command Guide.
- **Fax Commands** – The following guides provide fax developer information.
  - S000262 Fax Developer Guide Class 1 and Class 1.0
  - S000239 Fax Developer Guide Class 2 and Class 2.0/2.1

Chapter 2 – Mechanical Drawings

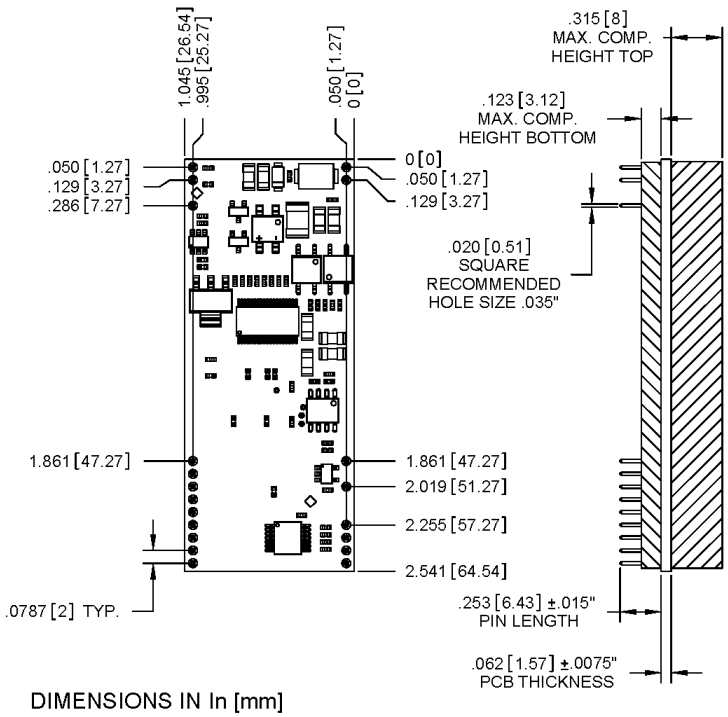
MT9234SMI-92, -L-92, and -HV-92 Builds





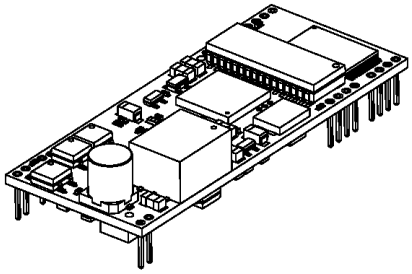


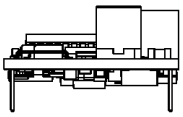
MT9234SMI-92
MT9234SMI-L-92
MT9234SMI-HV-92

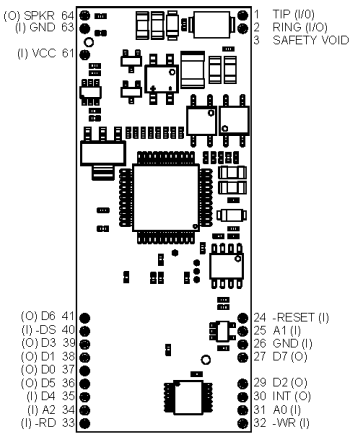


DIMENSIONS IN In [mm]

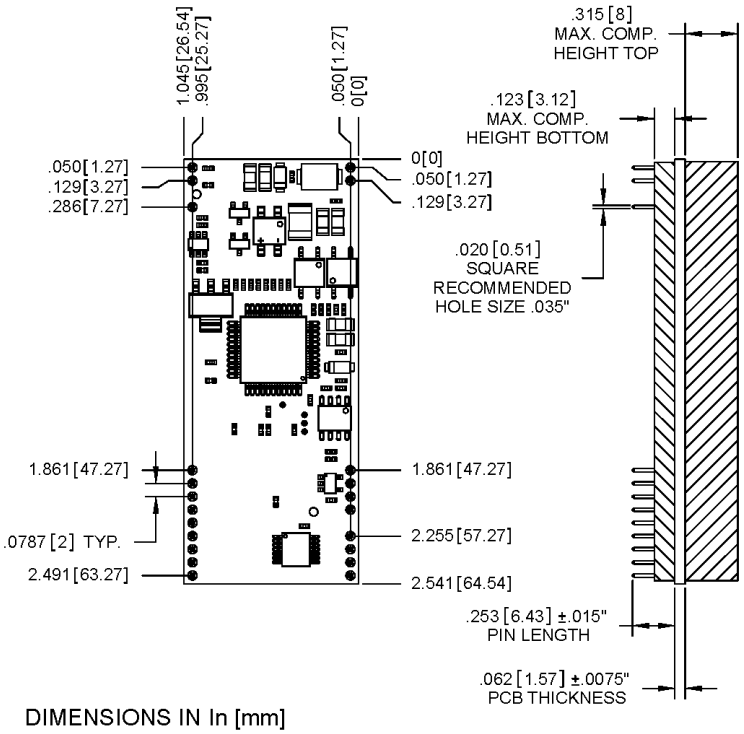
Parallel Builds







MT9234SMI-P-92
MT9234SMI-P-L-92
MT9234SMI-P-HV-92



DIMENSIONS IN In [mm]

Chapter 3 – Specifications

Technical Specifications

Category	Description
General	
Standards	V.92, V.34 enhanced, V.34, V.32bis, V.32, V.22bis, V.22; Bell 212A and Bell 103
Speed, Format, Compression	
Serial/Data Speeds	Serial port data rates adjustable to 300, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, and 230400 bps
Client-to-Client Data Rates	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, 2400, 1200, 0-300 bps
Data Format	Serial, or 8-bit parallel interface, asynchronous
Character Format	10 bit or 11 bit
Data Error Correction (ECM)	V.44; V.42 (LAPM, MNP 2-4)
Data Compression	V.42bis, MNP 5
Fax	
Fax Compatibility	V.17, V.29/V.27/V.21, V.34
Fax Class	Class 1 &1.0 – All builds Class 2, 2.0/2.1 – All builds
Fax Compression	MH, MR, MMR
Fax Error Correction Mode	ECM
Operation Modes	Fax online modes; full duplex over dial-up or 2-wire leased lines; data mode; command mode; online command mode; V.54 test mode
Physical Description	
Weight	0.6 oz. (0.017kg)
Dimensions	2.541” L x 1.045” W x 0.68” H (6.45cm L x 2.65cm W x 1.7cm H)
Environment	
Operating Temperature	-40° C to +85° C
Storage Temperature	-40° C to +85° C
Humidity	20% to 90% non-condensing
Power Requirements	
Operating Voltage	3.3V or 5V depending on build
Input Power	3.3V or 5V depending on build

Category	Description
Transmission	
Transmit Level	- 11 dBm (varies by country setting)
Receiver Sensitivity	- 43 dBm under worst-case conditions
DAA Isolation	1.5Kv r.m.s. or 2121 VDC at working voltage of 250VAC 2Kv r.m.s. or 2828 VDC at working voltage of 125VAC
Flow Control	XON/XOFF (software), RTS/CTS (hardware)
Command Buffer	60 characters
Telephony/TAM	TAM: S-101 AT+V commands (no CODEC for speakers/microphone interface)
Certifications, Compliance, Warranty	
EMC Compliance	FCC Part 15 Canadian EMC EN55022 EN55024 GB4943, GB9254
Safety Compliance	UL 60950 cUL 60950 EN 60950 AS/NZS 60950:2000 CCC For HV builds UL 60601-1 EN 60601-1
Warranty	Two years

Device Reset

The SocketModem is ready to accept commands after a fixed amount of time (“X” Time) after power-on or reset.

Model	Time Constant	"X" Time	Minimum Reset Pulse[1]
MT9234SMI	400 ms	6 seconds	100us

[1]The SocketModem may respond to a shorter reset pulse.

Modem Reset (with weak pull-up). The active low –RESET input resets the SocketModem logic and returns the AT command set to the original factory default values or to "stored values" in NVRAM.

DC Electrical Characteristics

Units: Volts 5VDC Characteristics (VDD = 5V ± 0.25V) VDDMAX = 5.25V
3.3VDC Characteristics (VDD = 3.3V ± 0.3V) VDDMAX = 3.6V

Parameter	Minimum	Maximum	
5V Serial – Standard (SMI) and medical device (SMI-HV) build options			
Digital Inputs –DTR (40), –TXD (35), –RTS (33)	Input High Min 2.52V	Input Low Max 0.9V	
–Reset (24)	Input High Min 2.52V	Input Low Max 0.3V	
Digital Outputs –DCD (39), –CTS (38), –DSR (37), –RI (36), –RXD (34)	Output High Min 2.3V	Output Low Max 0.4V	Current Drive 2mA
Digital Input Capacitance			5 pF
5V Parallel – Standard (SMI) and Medical Device (SMI-HV) Build Options			
Digital Inputs –DS (40)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Inputs (hysteresis input buffer) A0 (31), A1 (25), A2 (34), –WR (32), –RD (33)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Input / Output Output buffer can source 12 mA at 0.4 V DO (37), D1 (38), D2 (29), D3 (39), D4 (35), D5 (36), D6 (41), D7 (27)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Output INT (30)	Output High Min 2.3V	Output Low Max 0.4V	Current Drive 2mA
Digital Input Capacitance			5 pF
3.3V Serial – Industrial Temperature (SMI-L) Build Option			
Digital Inputs –DTR (40), –TXD (35), –RTS (33)	Input High Min 2.52V	Input Low Max 0.9V	
–Reset (24)	Input High Min 2.52V	Input Low Max 0.3V	
Digital Outputs –DCD (39), –CTS (38), –DSR (37), –RI (36), –RXD (34)	Output High Min. 2.3V	Output Low Max 0.4V	Current Drive 2mA
Digital Input Capacitance			5 pF
3.3V Parallel – Industrial Temperature (SMI-L) Build Options			
Digital Inputs –DS (40)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Inputs (hysteresis input buffer) A0 (31), A1 (25), A2 (34), –WR (32), –RD (33)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Input/Output Output buffer can source 12 mA at 0.4 V DO (37), D1 (38), D2 (29), D3 (39), D4 (35), D5 (36), D6 (41), D7 (27)	Input High Min 2.52V	Input Low Max 0.9V	
Digital Output INT (30)	Output High Min 2.3V	Output Low Max 0.4V	Current Drive 2mA
Digital Input Capacitance			5 pF

Pin Descriptions for a Parallel SocketModem Device

Pin #	Signal	I/O	Description
1	Tip	I/O	Tip Signal from Telco. Tip connection to the phone line (RJ-11 Pin 4). The SocketModem is Tip/Ring polarity insensitive.
2	Ring	I/O	Ring Signal from Telco. Ring connection to the phone line (RJ-11 Pin 3). The SocketModem is Tip/Ring polarity insensitive.
24	–RESET	I	Device Reset (with pull-up). The active low –RESET input resets the device logic and returns the configuration of the device to the original factory default values or "stored values" in the NVRAM. Refer to *Device Reset* for more information.
25	A1	I	Host Bus Address Line 0. During a host read or write operation, A0 selects an internal 16C450 or 16C550-compatible register. The state of the divisor latch access bit (DLAB) affects the selection of certain registers.
26	DGND	GND	Digital Ground
30	INT	O	Host Bus Interrupt. INT output is set high when the receiver error flag, receiver data available, transmitter holding register empty, or modem status interrupt have an active high condition. INT is reset low upon the appropriate interrupt service or master reset operation.
31	A0	I	Host Bus Address Line 1. During a host read or write operation, A1 selects an internal 16C450 or 16C550-compatible register. The state of the divisor latch access bit (DLAB) affects the selection of certain registers.
32	–WR	I	Host Bus Write. –WR is an active low, write control input. When –DS is low, –WR low allows the host to write data or control words into a selected modem register.
33	–RD	I	Host Bus Read. –RD is an active low, read control input. When –DS is low, –RD low allows the host to read status information or data from a selected modem register.
34	A2	I	Host Bus Address Line 2. During a host read or write operation, A2 selects an internal 16C450 or 16C550-compatible register. The state of the divisor latch access bit (DLAB) affects the selection of certain registers.
40	–DS	I	Host Bus Device Select. –DS input low enables the modem for read or write.
61	VCC	PWR	+5V or 3.3V Supply (depends upon model).
63	AGND	GND	Analog Ground. This is tied common with DGND on the SocketModem. To minimize potential ground noise issues, connect audio circuit return to AGND.
64	SPKR	O	Speaker. Dual purpose output for call progress signals or speakerphone functions. Call Progress on the MT9234SMI is an analog output.

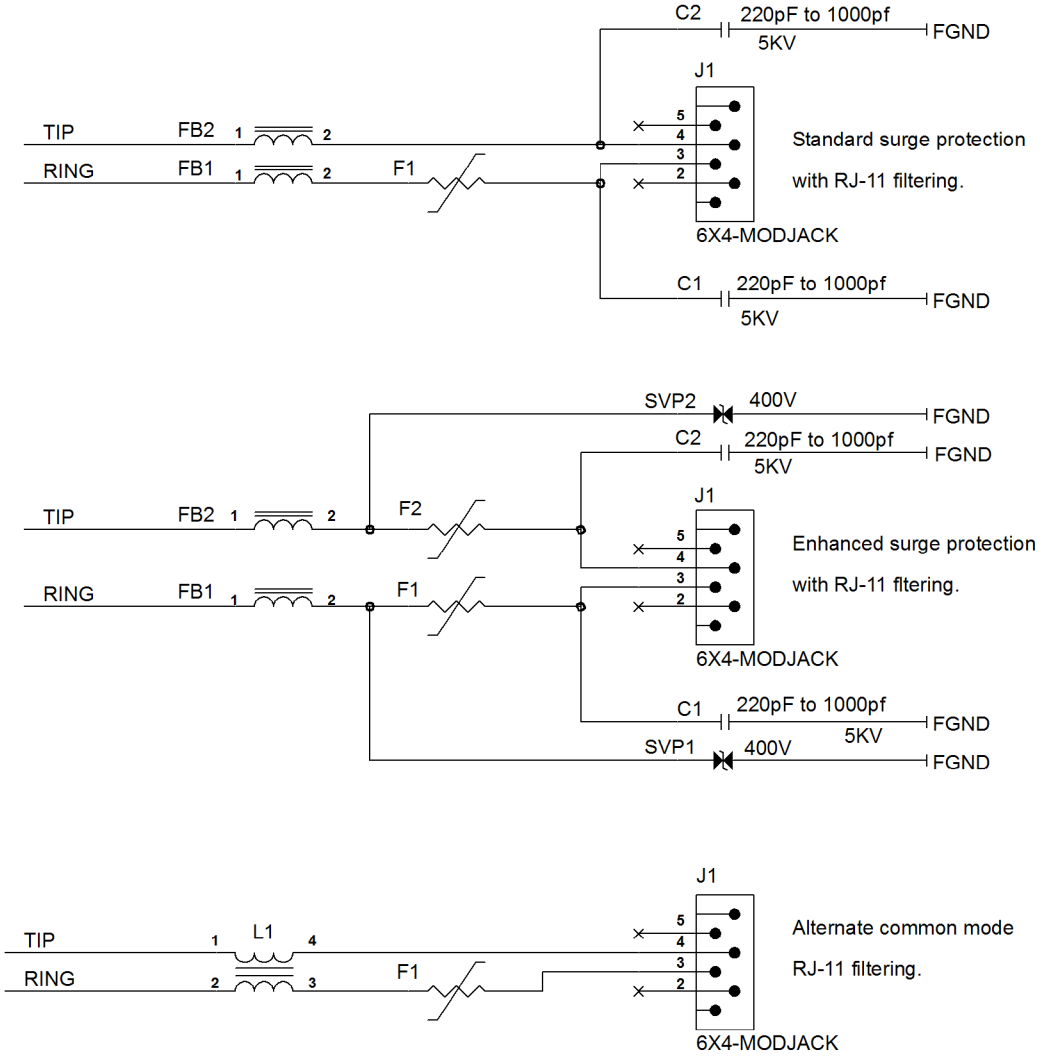
Power Measurements

Multi-Tech Systems, Inc. recommends that you incorporate a 10% buffer into your power source when determining product load.

	Sleep Mode	Typical	Maximum
MT9234SMI-L 3.3 Volt			
Current (AMPS)	0.081	0.114	0.122
Watts	0.264	0.373	0.397
MT9234SMI 5.0 Volt			
Current (AMPS)	0.082	0.116	0.122
Watts	0.409	0.579	0.606
MT9234SMI-P 3.3 Volt			
Current (AMPS)	0.079	0.112	0.116
Watts	0.260	0.366	0.378
MT9234SMI-P 5.0 Volt			
Current (AMPS)	0.079	0.114	0.119
Watts	0.394	0.567	0.589

Chapter 4 – Application Notes

Tip and Ring Interface



OEM Motherboard Filtering and Surge Protection Options
See Design Considerations and Recommended Parts in the Universal SocketModem Developer Guide.

Recommended Uses for Filtering Options

- **Enhanced Surge Protection with RJ-11 Filtering**
  Use this option when additional lightning protection may be needed.
- **Alternate Common Mode with RJ-11 Filtering**
  Use this option when your design has common mode emission issues.

Chapter 5 – Parallel Devices

Parallel Timing Requirements

Timing Requirements for Parallel Write

Parameter	Min	Max	Unit
–DS to –WR Setup (low to low)	10	-	ns
A0, A1, A2 to –WR Setup (valid to low)	15	-	ns
–WR Pulse Width (low to high)	40	-	ns
D0–D7 to –WR Setup (valid to high)	30	-	ns
–WR to –DS hold (high to high)	0	-	ns
–WR to A0–A2 Hold (high to invalid)	0	-	ns
–WR to D0–D7 Hold (high to invalid)	0	-	ns
–WR interaccess (high to low) Non-MIMIC Accesses MIMIC Accesses	 10 110	 - -	 ns ns

Timing Requirements for Parallel Read

Parameter	Min	Max	Unit
–DS to –RD Setup (low to low)	10	-	ns
A0, A1, A2 to –RD Setup (valid to low)	15	-	ns
–RD Pulse Width (low to high)	40	-	ns
–RD to –DS hold (high to high)	0	-	ns
–RD to A0–A2 Hold (high to invalid)	0	-	ns
–WR interaccess (high to low) Non-MIMIC Accesses MIMIC Accesses	 10 110	 - -	 ns ns

SocketModem Parallel Interface Internal Registers

The SocketModem parallel interface mimics a 16C550A UART. It is similar to the MIMIC interface used in the Zilog Z80189. The SocketModem mimic (MMM) uses this standard interface while replacing the serial to parallel data transfer with a parallel to parallel data transfer.

The MMM interface controls an 8-bit parallel data transfer that is interrupt driven. Interrupts usually indicate one or both of two conditions:

1. The receive (RX) FIFO has reached a trigger level or time-out condition and needs to be emptied.

and/or

2. The transmit (TX) FIFO is empty and waiting for more data from the Host.

Interrupts can also be triggered by a change in the modem status register (such as loss of carrier) or by errors in the line status register (overrun, parity, framing, break detect).

In addition to receive and transmit FIFOs, there are twelve other control/status registers called the MMM register set that can be accessed through this interface.

SocketModem MIMIC (MMM) Operation

Data flow through MMM is bi-directional. Data can flow from the host through the transmit FIFO to the SocketModem control and from the SocketModem controller through the receive FIFO to the Host simultaneously.

In the receive path, 8-bit data is received asynchronously from the SocketModem controller by the receive FIFO where it is stored with associated three error bits. The error bits must arrive via a SocketModem controller I/O write to MMM shadow line status register before the actual data bits. The error bits are temporarily stored so they may be written, with associated data bits, to the 11-bit wide RX FIFO.

The RX FIFO write pointer increments after every data write. RX FIFO trigger levels, data ready signal, and time-out counter are checked to see if a Host-interrupt needs to be sent. The data ready signal will be activated and the MMM is ready to accept data.

After every data write, the RX FIFO write pointer is incremented. RX FIFO trigger levels, data ready signal, and time-out counter are checked to see if a Host-interrupt needs to be sent. The data ready signal will be activated and MMM sits poised to accept another data word.

We recommend that the host:

1. Read the MMM IIR register to determine the interrupt type.
2. Check LSR bit 7 to see if there are any data errors residing in the receive FIFO.
3. Either:
   a. Alternately read a data word through the RX FIFO read pointer and the error bits via the MMM LSR until the FIFO is empty

   or

   b. Read successive data words (knowing there were no errors in the FIFO) until the trigger count is met.

A similar sequence occurs when data flows from host through transmit FIFO, except there is no error bit manipulation/checking involved.

FIFO Operation

The FIFO Control Register (FCR) bit-0 enables the 16-byte transmit and receive data FIFOs. You can set the receive trigger level via FCR bits 6/7. The receiver FIFO section includes a time-out function to ensure data is delivered to the external host. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read after the loading of a character or the receive trigger level has been reached.

Receive (RX) FIFO

You can configure the RX FIFO to be 16 words deep and 11 bits wide. Each word consists of 8 data bits and 3 error bits. The MMM RX block contains read and write pointers and status flag circuitry that need only be presented with data for input, reset, read/write control signals, and read/write clock signals. The MMM Rx block internally manages the FIFO register file and pointers, and provides simultaneous read/write capability (no contention problems).

The MMM RX block provides data for output, the FIFO full flag, FIFO empty flag, and an almost full flag which uses an associated predefined trigger level (obtained from the MMM FCR control register) to signal when the trigger level has been met. Select four possible trigger levels by programming bits 6-7 of the FCR control register.

A typical interrupt driven write to the RX block is a two-step process. First, the MMM micro-controller must write the 3 error bits to a shadow MMM LSR status register. Then, the micro-controller writes the data to the RX FIFO. During this write operation, the 3 error bits are loaded directly from the LSR shadow register into bits 8-10 of the selected 11-bit wide FIFO register. These error bits represent the parity error, framing error, and break interrupt signals associated with each data work transmission into the receive FIFO. When the receive FIF is read, these error bits are loaded directly into bits 2-4 of the MMM LSR register.

A2	A1	A0	Register Name	Register Description	Host Access
0	0	0	RBR	Receive Buffer (RX FIFO)	DLAB = 0 R only
0	0	0	THR	Transmit Holding (TX FIFO)	DLAB = 0 W only
0	0	1	IER	Interrupt Enable	DLAB = 0 R/W
0	1	0	IIR	Interrupt Identification	DLAB = X R only
0	1	0	FCR	FIFO Control	DLAB = X W only
0	1	1	LCR	Line Control	DLAB = X R/W
1	0	0	MCR	Modem Control	DLAB = 0 R/W
1	0	1	LSR	Line Status	DLAB = X R only
1	1	0	MSR	Modem Status	DLAB = X R only
1	1	1	SCR	Scratch pad	DLAB = 0 R/W
0	0	0	DLL	LSB of Divisor Latch	DLAB = 1 R/W
0	0	1	DLM	MSB of Divisor Latch	DLAB = 1 R/W
1	1	1	DLX	Divisor Latch	DLAB = 1 R/W
1	0	0	MCX	Status/Control	DLAB = 1 R/W

Notes

The General Register set is accessible only when DS is a logic 0.

The Baud Rate register set is accessible only when DS is a logic 0 and LCR bit-7 is a logic 1.

Time Out Interrupts

IER bits 0-3 enable the interrupts. Following a reset, the transmitter interrupt is enabled. The SocketModem will issue an interrupt to indicate that the transmit holding register is empty. This interrupt must be serviced before continuing operations.

The LSR register provides the current singular highest priority interrupt only. A higher priority interrupt may mask lower priority interrupt(s). Only after servicing the higher pending interrupt will the lower priority interrupt(s) appear in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors. When two interrupt conditions have the same priority, it is important to service these interrupts correctly.

When enabled by IER bit-3, Receive Data Ready and Receive Time Out have the same interrupt priority. The receiver issues an interrupt after the number of characters received reaches the programmed trigger level. In this the MMM FIFO may hold more characters than the programmed trigger level. After removing a data byte, re-check the LSR bit-0 for additional characters. If the receive FIFO is empty, a Receive Time Out will not occur. The time out counter is reset at the center of each stop bit received or each time the Receive Holding Register (RHR) is read.

Register Functional Definitions

The following table and descriptions define the assigned bit functions for the twelve internal registers.

Internal Registers

A2	A1	A0	Register [Default][1]	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set: [2]											
0	0	0	RBR [XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	0	THR [XX]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	1	IER [00]	0	0	0	0	Modem Status Interrupt	Receive Line Status interrupt	Transmit Holding Register interrupt	Receive Holding Register interrupt
0	1	0	IIR [XX]	FIFO enable	FIFO enable	0	0	Interrupt ID	Interrupt ID	Interrupt ID	Interrupt Pending
0	1	0	FCR [00]	RX Trigger (MSB)	RX trigger (LSB)	Detect change in FCR	TX FIFO overrun bit	0	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0	1	1	LCR [00]	Divisor latch access (DLAB)	Set break	Stick parity	Even parity	Parity enable	0	Word length bit-1	Word length bit-0
1	0	0	MCR [00]	0	0	0	0	INT enable	OUT 1	-RTS	-DTR
1	0	1	LSR [60]	RX FIFO data error	TX empty THR empty	THR Empty	Break interrupt	Framing error	Parity error	Overrun error	Receive data ready
1	1	0	MSR [X0]	CD	RI	DSR	CTS	Delta -CD	Delta -RI	Delta -DSR	Delta -CTS
1	1	1	SCR [FF]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
Special Register Set[3]											
0	0	0	DLL [00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	1	DLM [00]	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

Notes:

[1] The value between the square brackets represents the register's initialized HEX value, X = N/A.

[2] The General Register set is accessible only when DS is a logic 0.

[3] The Baud Rate register set is accessible only when DS is a logic 0 and LCR bit-7 is a logic 1.

RBR – Receive Buffer (RX FIFO)

All eight bits are used for receive channel data (host read/data in; host write/data out). The three error bits per byte are copied into bits 2, 3, and 4 of the LSR during each host I/O read; therefore, they are available for monitoring on a per-byte basis.

THR – Transmit Holding Register (TX FIFO)

All eight bits are used for transmit channel data (host write/data out; host read/data in).

IER – Interrupt Enable

Bits 4–7 Reserved and will always read 0.
Bits 0-3 Set by host software only and cleared by software control or host reset.
Bit 3 Enables modem status IRQ. If bits 0–3 of the MSR are set and this bit is set to 1 (enabled), a host interrupt is generated.
Bit 2 Enables receive line status IRQ. If bits 1–4 (overrun, parity, framing, break errors) of the LSR are set and this bit is set to a logic 1, a host interrupt is generated.
Bit 1 Enables transmit holding register IRQ. If bit 5 (transmit holding register empty) of the LSR is set and this bit is set to a 1, a host interrupt is generated.
Bit 0 Enables received data available IRQ. If bit 0 (data ready) of the LSR is set and this bit is set to a 1, a host interrupt is generated.

IIR – Interrupt Identification (Read Only)

Bits 6–7 (FIFO enabled bits). These bits will read a 1 if FIFO mode is enabled and the 16450 enable bit is 0 (no force of 16450 mode).
Bits 4–5 Reserved and always read a 0.
Bits 1–3 Interrupt ID bits.
Bit 0 Interrupt pending. If logic 0 (in default mode), an interrupt is pending.

When the host accesses IIR, the contents of the register are frozen. Any new interrupts will be recorded, but not acknowledged during the IIR access. This requires buffering bits (0–3, 6–7) during IIR reads.

Interrupt Sources and Reset Control Table

Bit 3	Bit 2	Bit 1	Priority	Interrupt Source	Interrupt Reset Control
0	1	1	Highest	Overrun, parity, framing, error or break detect bits set by SocketModem Controller	Reading the LSR
0	1	0	2nd	Received data trigger level	RX FIFO drops below trigger level
1	1	0	2nd	Receiver time-out with data in RX FIFO	Read RX FIFO
0	0	1	3rd	TX holding register empty	Writing to TX holding register or reading IIR when TX holding register is source of error
0	0	0	4th	MODEM status: CTS, DSR, RI or DCD	Reading the MSR

FCR – FIFO Control

Bits 7-6	Used to determine RX FIFO trigger levels.
Bit 5	Used to detect a change in the FCR.
Bit 4	TX FIFO overrun bit.
Bit 3	DMA mode select. Must be set to zero. When bit 3 is a 0, the 16450 mode is enabled which does only single-byte transfers.
Bit 2	TX FIFO reset. This will cause TX FIFO pointer logic to be reset (any data in TX FIFO will be lost). This bit is self clearing; however, a shadow bit exists that is cleared only when read by the host, thus allowing the host to monitor a FIFO reset.
Bit 1	RX FIFO reset. This will cause RX FIFO pointer logic to be reset (any data in RX FIFO will be lost). This bit is self clearing; however, a shadow bit exists that is cleared only when read by the host, thus allowing the host to monitor a FIFO reset.
Bit 0	FIFO enable. The host writes this bit to logic 1 to put the block in FIFO mode. This bit must be a 1 when writing other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFOs or the RBR and THR registers will be lost and any pending interrupts are cleared.

Bit 7	Bit 6	16 Deep FIFO Trigger Levels (# of bytes) Default
0	0	1
0	1	4
1	0	8
1	1	14

LCR – Line Control

Bit 7	Divisor latch access bit. This bit allows the host, access to the divisor latch. Under normal circumstances, the bit is set to 0 (provides access to the RX and TX FIFOs at address 0). If the bit is set to 1, access to transmitter, receiver, interrupt enable, and modem control registers is disabled. In this case, when an access is made to address 0, the divisor latch least (DLL) significant byte is accessed. Address 1 accesses the most significant byte (DLM). Address 7 accesses the DLX divisor latch register. Address 4 accesses the MCX status/control register.
Bit 6	Used to denote a host-generated set break condition.
Bits 0,1,3,4,5	Used only in parity bit generation for the 7 bit data byte case. Bits 0 and 1 are used for word length select (b0 = 0 and b1 = 1 is used for 7 bit data). Bit 3 is parity enable. Bit 4 is even parity select. Bit 5 is stick parity.

MCR – Modem Control

Bits 5-7	Reserved, and will always be 0
Bit 3	Controls the signal used to 3-state the host interrupt. If 0, then an active-low L33xV output will be set to 0, and this signal will be used to 3-state the host interrupt output pin.
Bits 2-0	Reserved.
Bit 2	OUT1.
Bit 1	Request to Send (RTS).
Bit 0	Data terminal ready (DTR).

LSR – Line Status

Bit 7	Error in RX FIFO. This bit is always set to 1 if at least one data byte in the RX FIFO has an error. This will clear when there are no more errors in the RX FIFO.
Bit 6	Transmitter empty. This bit is the same as LSR bit 5 (THRE) in MMM
Bit 5	Transmitter holding register empty. This bit is set to 1 when either the transmitter holding register has been read (emptied) by the micro-controller (16450 mode) or the TX FIFO is empty (16550 mode). This bit is set to 0 when either the THR or the TX FIFO becomes not empty in 16450 mode. In 16550 mode, it is set to 0 only after the trigger level has been met since the last occurrence of TX FIFO empty. If the transmitter timer is enabled, a shadow bit exists which delays the timer setting this bit to 1. When reading this bit, the micro-controller will not see the delay. Both shadow and register bits are cleared when the host writes to the THR or TX FIFO in 16450 mode. The trigger level must be reached to clear the bit in 16550 (FIFO) mode.
Bits 4-2	Used for parity error, framing error, and break detect. These bits are written, indirectly, by the micro-controller as follows: The bits are first written to the shadow bit locations when the micro-controller write accesses the LSR. When the next character is written to the receive buffer (RBR) or the RX FIFO, the data in the shadow bits is then copied to the RBR (16450 mode) or RX FIFO (16550 mode). In FIFO mode, bits become available to the host when the data byte associated with the bits is next to be read. In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the micro-controller writes to the RBR or RX FIFO, the shadow bits are auto cleared. The register bits are updated with each host read
Bit 1	Overrun error. This bit is set if the micro-controller makes a second write to RBR before the host reads data in the buffer (16450 mode) or with a full RX FIFO (16550 mode). No data will be transferred to the RX FIFO under these circumstances. This bit is reset when the host reads the LSR.
Bit 0	Data ready bit. This bit is set to 1 when received data is available, either in the RX FIFO (16550 mode) or the RBR (16450 mode). This bit is set immediately upon the micro-controller writing data to the RBR or FIFO if the receive timer is not enabled, but it is delayed by the timer interval if the receive timer is enabled. For micro-controller read access, a shadow bit exists so that the micro-controller does not see the delay that the host sees. Both bits are cleared to logic 0 immediately upon reading all data in either RBR or RX FIFO.

MSR – Modem Status

Bits 4 through 7 of the MSR can also take on the MCR bits 0 through 3 value when in MCR loop mode (i.e. when MCR b4 = 1). The transfer of bits in loop back has a null modem twist (i.e. MCR b0 goes to MSR b5 and MCR b1goes to MSR b4).

Bit 7	Data carrier detect (DCD) bit.
Bit 6	Ring indicator (RI) bit.
Bit 5	Data set ready (DSR) bit.
Bit 4	Clear to send (CTS) bit.
Bit 3	Delta data carrier detect pin. This bit is set to a 1 whenever the data carrier detect bit changes state. It is reset when the host reads the modem status register.
Bit 2	Trailing edge ring indicator bit. This bit is set to 1 on the falling edge of the ring indicator bit. It is reset when the host reads the modem status register.
Bit 1	Delta data set ready bit. This bit is set to 1 whenever the data set ready changes state. It is reset when the host reads the modem status register.
Bit 0	Delta clear to send bit. This bit is a one whenever the clear to send bit changes state. It is reset when the host reads the modem status register.

SCR – Scratch

The host programmer uses this register for temporary data storage.

DLL – Divisor Latch (LSByte)

This register contains low-order byte for the 16-bit clock divider. It is kept to maintain register set compatibility with the 16C550A interface. However, it is not used for clock generation since MMM does not require the generation of a real baud clock.

DLM – Divisor Latch (MSByte)

This register contains high-order byte for the 16-bit clock divider. It is kept to maintain register set compatibility with the 16C550A interface. However, it is not used for clock generation, since MMM does not require the generation of a real baud clock.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in the Table below shows the selectable baud rates available when using a 1.8432 MHz external clock input.

Baud Rate Generator Programming Table

Baud Rate	16 x Clock Divisor (Decimal)	DLM Value (HEX)	DLL Value (HEX)
110	1047	04	17
300	384	01	80
600	192	00	C0
1200	96	00	60
2400	48	00	30
4800	24	00	18
9600	12	00	0C
19.2K	6	00	06
38.4K	3	00	03
57.6K	2	00	02
115.2K	1	00	01