产品规格书

Product specifications

型号 model QMDS160160V02AKW

修订记录

编号	修订内容	日期	版本
1	新文件生成		V.1

修订		审核	
日期		日期	

目录

contents

1. 基本参数

类型	规格	说明
主要硬件	LCD 液晶屏+LED 背光+铁框+PCB 驱动电路(SMT)	
显示模式	FSTN 正向显示，白底色黑字	
显示类型	半透型 LCD+白色背光	
物理分辨率	160×160	
外形尺寸（mm）	84.0×84.0×8.50	
可视区尺寸（mm）	62.30×62.40	
DOT 点尺寸（mm）	0.335×0.335	
DOT 点间距（mm）	0.35×0.35	
视角	6 O'clock	12O'clock可选
占空比（Duty）	1/160	
偏压比（Bias）	1/10	
控制器	UC1698U	
接口类型	8位并口，串口,插接	
模块电压	3.3V/5.0V	
工作温度（℃）	-20~+70	
存储温度（℃）	-30~+80	

2. 结构尺寸图纸

2-1 产品实物图片

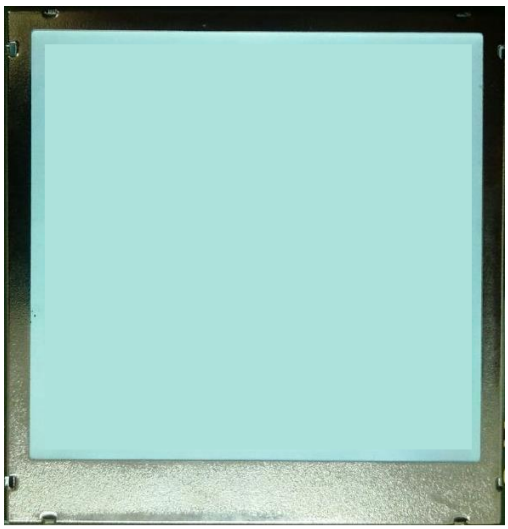


图 1.实物图片

2-2 结构尺寸图纸内容

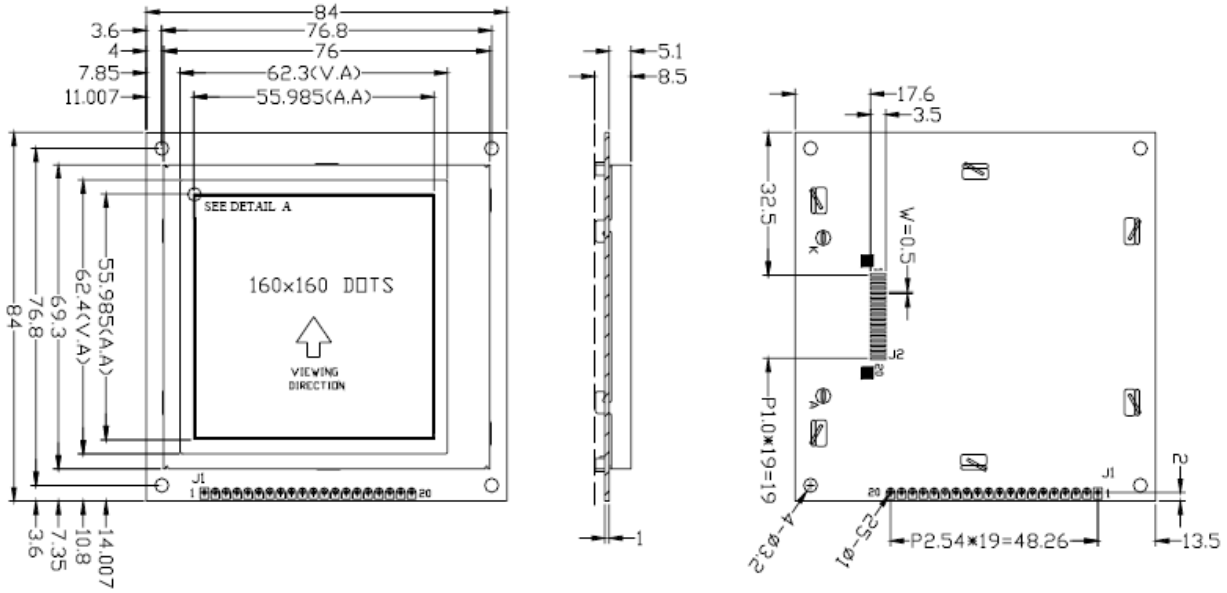


图 2.产品结构图纸

3. 原理图

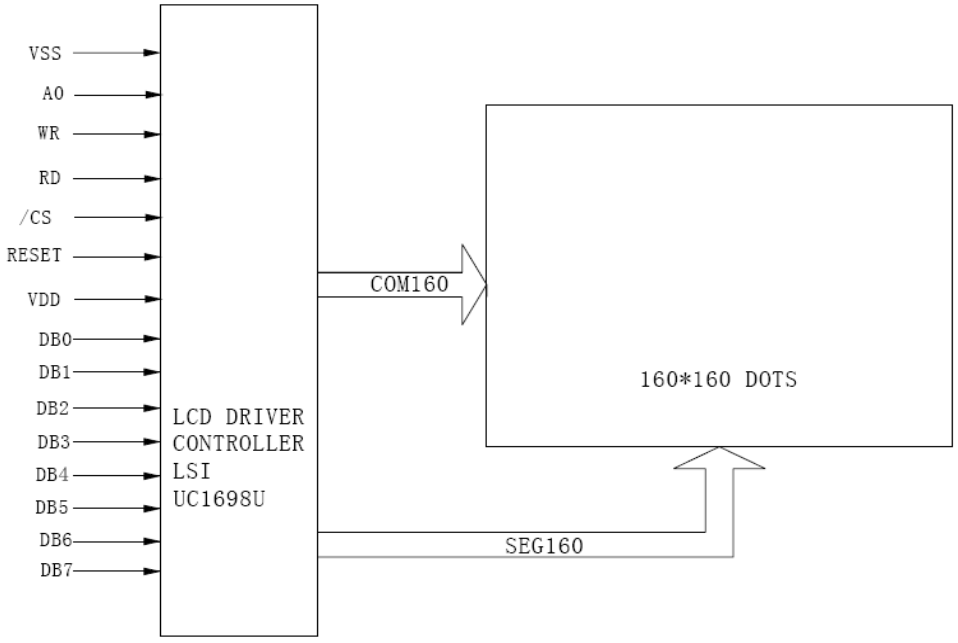


图 3.显示原理图

4. 极限参数值

4-1 极限电压参数

Item	Symbol	Min	Max	Unit	Note
电源电压	Vdd-Vss	-0.3	5.0	V	
LCD 驱动电压	Vdd-Vee	8.0	18.0	V	
I/O 口输入电压	-	Vss	Vdd	-	

4-2 极限环境参数

Item	Min	Max	Unit	Note
工作温度	-20	70	℃	
存储温度	-30	80	℃	
环境湿度	-	90	%RH	

5. 光电特性

5-1 模组电特性参数

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
逻辑电压	Vdd	----	2.7	3.3	5. 0	V	
LCD 驱动电压	Vdd-Vo	----	16	16.5	17	V	
输入电压	VIH	----	2.0	---	Vdd	V	
	VIL	----	Vss	---	0.8	V	
频率	FELM	Vdd=5V	65	78	85	Hz	

5-2 背光电特性参数

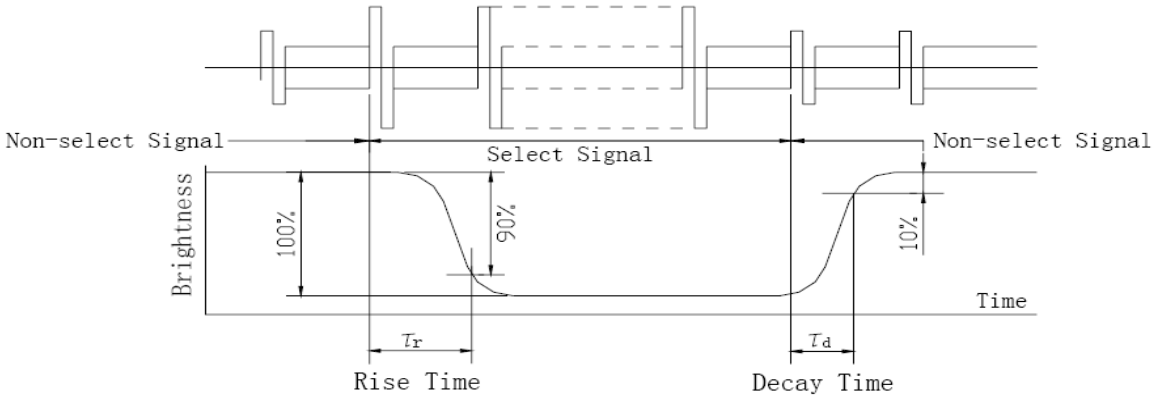
Item	Symbol	Min	Typ	Max	Unit	Condition	Note
正向电压	Vf	2.8	3.0	3.2	V	If=70mA	

5-3光特性参数（测试环境25℃）

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Viewing angle	θ	K≧2.0 Φ	40	---	---	deg	
Contrast ration	K	θ =5o Φ	---	5	---	---	
Response	Tr	θ =5o Φ	---	100	120	ms	
Response time(fall)	Tf	θ =5o Φ	---	60	80	ms	

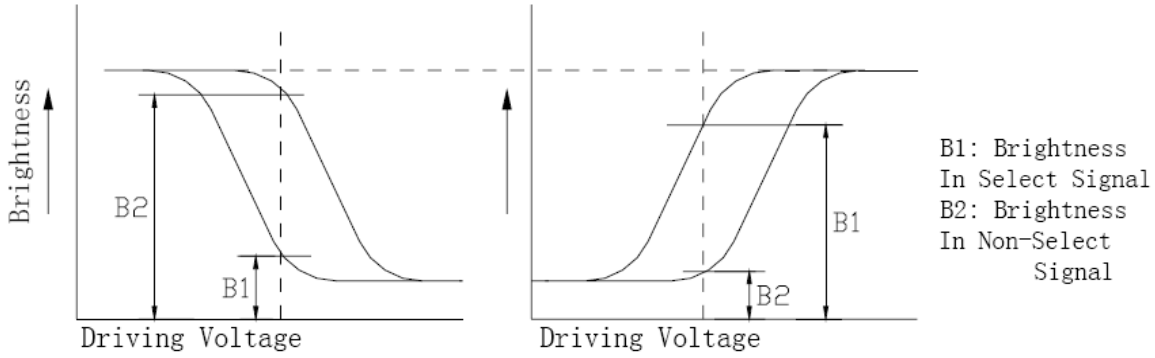
5-4 光学特性测定方法

● Definition of Optical Response Time



In case of Negative type,
wave from of changing brightness becomes reverse
(Non Select Signals:0%, Select Signals:100%

● Definition of Contrast Ratio(CR)

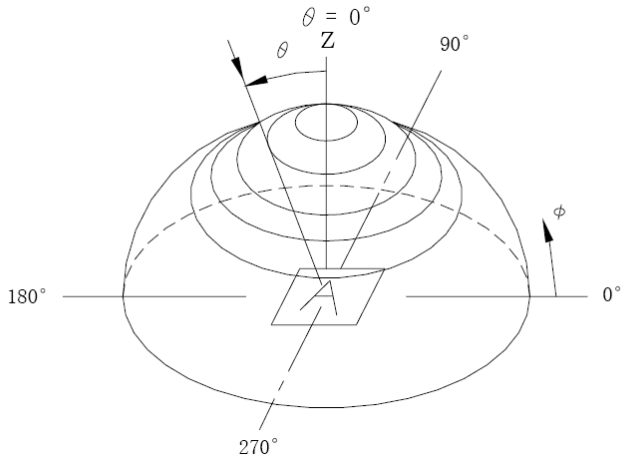


B1: Brightness In Select Signal
B2: Brightness In Non-Select Signal

$$CR=\frac{\text{Brightness In Non-Select Signal}}{\text{Brightness In Select Signal}}$$ (Positive Type)

$$CR=\frac{\text{Brightness In Select Signal}}{\text{Brightness In Non-Select Signal}}$$ (Negative Type)

● Definition of Viewing Angle θ and φ



6.接口定义及说明

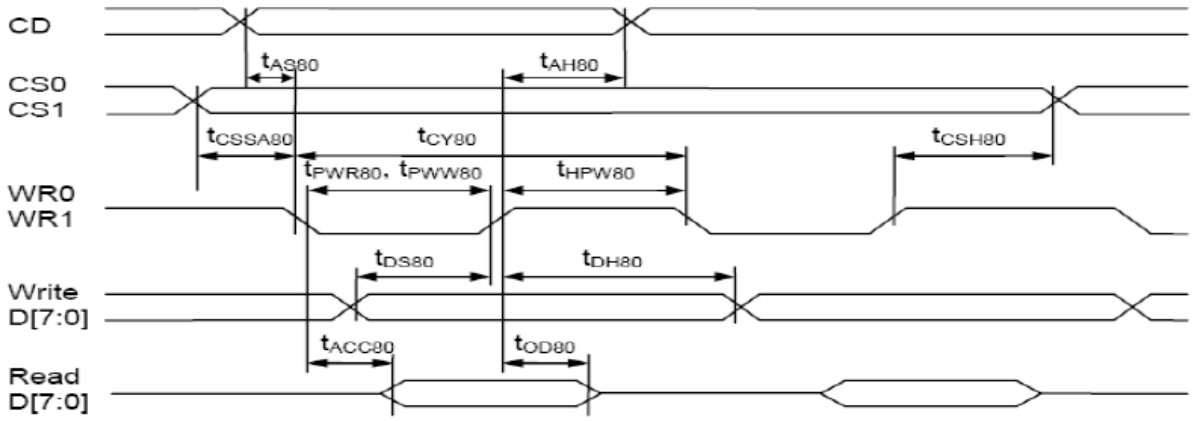
6-1 数据接口

Pin	Symbo	Level	Function	Note
1	FG	------	铁壳地	
2	VDD	3.3V	逻辑电源正	
3	VSS	0V	逻辑电源地	
4	P/S	H/L	0:并口.1: 串口,	
5	C86	H/L	1:6800/8BIT;0:8080/8BIT; 串口时:1:三线串口 S9,0:四线串口 S8	
6	/CS	L	LCD 选通信号，低有效	
7	CD	H/L	命令数据选择端，高电平：数据，低电平：命令	
8	WR1	H/L	80 时序时作为读信号，68 时序时作为使能信号，下降沿锁存；串行方式时接 VSS。	
9	WR0	H/L	80 时序时作为写信号；68 时序时是读或写信号选择端，串行方式接 VSS	
10	/RST	L	复位信号，低有效	
11	DB0	H/L	数据信号线 0	
12	DB1	H/L	数据信号线 1	
13	DB2	H/L	数据信号线 2	
14	DB3	H/L	数据信号线 3	
15	DB4	H/L	数据信号线 4	
16	DB5	H/L	数据信号线 5	
17	DB6	H/L	数据信号线 6	
18	DB7	H/L	数据信号线 7	
19	LED+	3.3V	背光电源正端	
20	LED-	0V	背光电源负端	

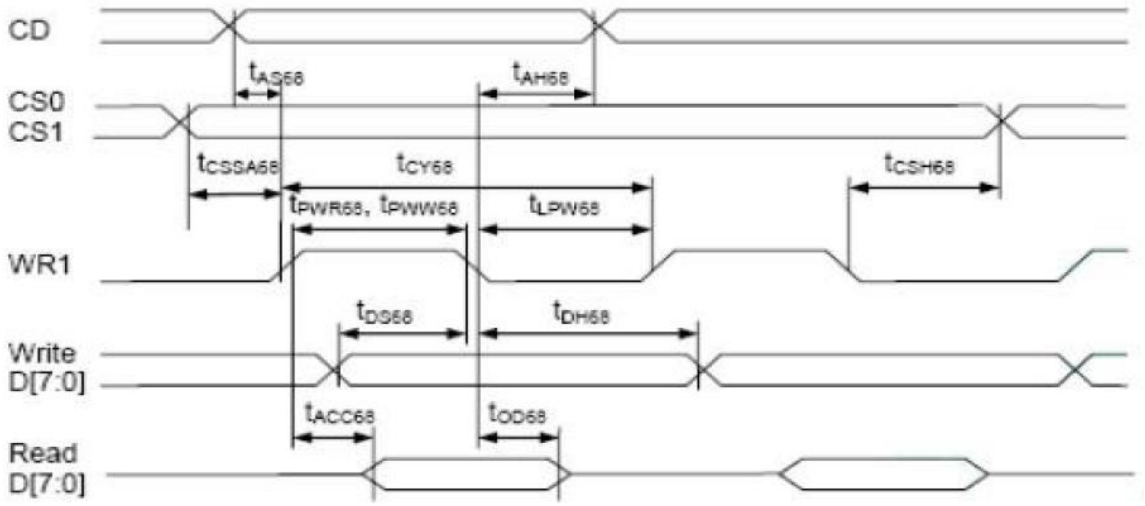
PIN	8080/8位	6800/8位	四线串口	三线串口
P/S	0	0	1	1
C86	0	1	0	1
/CS	/CS	/CS	/CS	/CS
CD	CD	RS	CD	0
WR1	RD	E	0	0
WR0	WR	R/W	0	0

6-2 时序图

6-2-1MPU 读/写时序(8080 时序)



6-2-2MPU读/写时序(6800时序)



6-2-3MPU 时序表

ITEM	SYMBOL	CONDITION	MIN.	MAX.	UNIT
C/D SET UP TIME	t_{CDS}	VDD=3.3V VSS=0V TA=25℃	0		ns
C/D HOLD TIME	t_{CDH}		0		
C/D, RD, WR PULSE WIDTH	t_{CE}, t_{RD}, t_{WR}		50		
DATA SET UP TIME	t_{DS}		30		
DATA HOLD TIME	t_{DH}		0		
ACCESS TIME	t_{ACC}		-	60	
OUTPUT HOLD TIME	t_{OH}		15	30	

7. MPU 指令说明

7-1 Display control instruction

UC1698u contains registers which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, starting with a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register.
Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after *Power-Up-Reset* and *System-Reset*.

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (159 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 10b: 11 **11b: 12**
TC	2	0H	Temperature Compensation (per °C) **00b: -0.00%** 01b: -0.05% 10b: -0.15% 11b: -0.25%
PM	8	40H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1b: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0b: The effective PM value, PMV = PM + PMO[5:0]
PC	2	2H	Power Control. PC[0]: **0b: LCD ⩽ 13nF** 1b: 13nF < LCD ⩽ 22nF PC[1]: 0b: External V_{LCD} **1b: Internal V_{LCD}** (10x charge pump)
AC	4	1H	Address Control. AC[0]: WA: Automatic column/row Wraparound (Default **1 : ON**) AC[1]: Auto-Increment order **0b : Column (CA) first** 1b : Row (RA) first AC[2]: RID: RA (row address) Auto Increment Direction (L : +1 H : -1) AC[3] : Window Program Mode **0b : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0) and (WPC1,WPP1) 1b : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0) and (WPC1,WPP1)

Name	Bits	Default	Description
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4]: Green Enhance Mode. *Only valid in 4K-color mode.* 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	9	090H	LCD Control: LC[0]: Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **0: OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **0: OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **0: OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 25.2. Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps Line Rate (for On/Off mode) 00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 64K color mode.** 5R-6G-5B (16-bit/RGB) when DC[4]=0: 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 64K color mode. 5R-6G-5B (16-bit/RGB) LC[8] : Partial Display Control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	5	1DH	N-Line Inversion: NIV[2:0]: 000b: 11 lines 001b: 19 lines 010b: 21 lines 011b: 25 lines 100b: 29 lines **101b: 31 lines** 110b: 37 lines 111b: 43 lines NIV[3]: 0b: no-XOR **1b: XOR** NIV[4]: 0b: Disable NIV **1b: Enable NIV**
CSF	3	0H	COM Scan Function CSF[0]: Interlace Scan Function **0b: LRM sequence: AEBCD-AEBCD** 1b: LRM sequence: AEBCD-EBCDA CSF[1]: FRC function **0: Disable FRC** 1: Enable FRC CSF[2]: Shade-1 / Shade-30 option **0: Dither directly on input data (SRAM Change)** 1: PWM (Pulse-width modulation) on SEG output stage

Name	Bits	Default	Description
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	8	00H	Window program starting row address. Value range: 0~159.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	8	9FH	Window program ending row address. Value range: 0~159
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000 : Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	7	--	Multiple-Time Programming. For V_{LCD} fine tune.
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

7-2 指令表

COMMAND TABLE

The following is a list of host commands supported by UC1698u

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
#: Useful Data bits –: Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver	PMO[6:0]								
				Product Code (8h)				PID[1:0]		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set APC[R][7:0], R = 0 or 1	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	40H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
		0	0	#	#	#	#	#	#	#	#		
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0
19	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[4:0]	1DH
				-	-	-	#	#	#	#	#		
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
28	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	159
		0	0	-	#	#	#	#	#	#	#		
30	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Shared with MTP commands: Set WPC0	0
		0	0	-	#	#	#	#	#	#	#		
31	Set Window Program Starting Row Address	0	0	1	1	1	1	0	1	0	1	Set WPP0	0
		0	0	#	#	#	#	#	#	#	#		
32	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0	Set WPC1	127
		0	0	-	#	#	#	#	#	#	#		
33	Set Window Program Ending Row Address	0	0	1	1	1	1	0	1	1	1	Set WPP1	159
		0	0	#	#	#	#	#	#	#	#		
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside
35	Set MTP Operation control	0	0	1	0	1	1	1	0	0	0	Set MTPC[4:0]	10H
		0	0	-	-	-	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
36	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[6:0] MTPM1[1:0]	0
		0	0	-	#	#	#	#	#	#	#		
		0	0	-	-	-	-	-	-	#	#		
37	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program commands: Set MTP1	N/A
		0	0	#	#	#	#	#	#	#	#		
38	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1	Set MTP2	N/A
		0	0	#	#	#	#	#	#	#	#		
39	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0	Set MTP3	N/A
		0	0	#	#	#	#	#	#	#	#		
40	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1	Set MTP4	N/A
		0	0	#	#	#	#	#	#	#	#		

NOTE:

- All other bit patterns other than commands listed above may result in undefined behavior.
- The interpretation of commands (36)~(40) depends on the setting of register MTPC[3].
  - Commands (37)~(40) are shared with commands (30)~(33). These two sets of commands share exactly the same code and control registers. When MTPC[3]=0, they are interpreted as Window Program commands and registers. When MTPC[3]=1, they function as MTP Control commands and registers.
- After MTP ERASE or PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.
- Under 16-bit bus mode and CD=0, D[15:8] is ignored and only D[7:0] is used. As a result, the bus cycles for commands under 16-bit bus and 8-bit bus are the same, and double-byte commands still need two bus cycles under 16-bit bus mode.

  Example:

  8-bit bus mode:

  Set PL[1:0] = 2'b11 : D[7:0] = 0010 1011

  Set PM[7:0] = 8'h8b : 1st D[7:0] = 1000 0001

  2nd D[7:0] = 1000 1011

  16-bit bus mode:

  Set PL[1:0] = 2'b11: D[15:0] = 0000 0000 0010 1011

  Set PM[7:0] = 8'h8b: 1st D[15:0] = 0000 0000 1000 0001

  2nd D[15:0] = 0000 0000 1000 1011

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data written to SRAM							

UC1698u will convert input RAM data to 16-bit of RGB data. Please refer to command `Set Color Mode` for detail of data-write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Each RGB triplet is stored as 16-bit in the display RAM. Each 16-bit of RGB data takes 1 (/ 2) RAM read cycles for 16 (/ 8) –bit bus mode, respectively. The read out RGB data is *after-extension* for 64K color mode.

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1st 8-bit Read								2nd 8-bit Read							

Write/Read Data Byte (commands (1) and (2)) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing commands `Set Row Address` and `Set Column Address`. If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

For 8-bit / 16-bit interface, the first 1 byte / 2 bytes of read, respectively, is a dummy read. Please ignore the data read out.

(3) GET STATUS & PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	GE	MX	MY	WA	DE	WS	MD	MS
	0	1	Ver	PMO[6:0]						
	0	1	Product Code				PID[1:0]		MID[1:0]	

Status1 definitions:
GE : Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.
MX : Status of register LC[1], mirror X.
MY : Status of register LC[2], mirror Y.
WA : Status of register AC[0]. Automatic column/row wrap around.
DE : Display enable flag. DE=1 when display is enabled
WS : MTP Operation succeeded
MD : MTP Option (1 for MTP version, 0 for non-MTP version)
MS : MTP action status

Status2 definitions:
Ver : IC Version Code. 0 or 1.
PMO[6:0] : PM offset value.

Status3 definitions:
Product Code : 1000b (8h)
PID[1:0] : Provide access to ID pins connection status.
MID[1:0] : LCM manufacturer's configuration.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	0	0	0	1	0	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: **0~127**

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b = -0.00%/^{o}C 01b = -0.05%/^{o}C 10b = -0.15%/^{o}C 11b = -0.25%/^{o}C

(6) SET POWER CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[0] according to the capacitance loading of LCD panel.

Panel loading definition: **0b : LCD ⩽ 13nF** 1b : 13nF < LCD ⩽ 22nF

Set PC[1] to program the build-in charge pump stages. Before changing PC[1] value, always ensure the IC is in a RESET state. Avoid changing PC[1] when the display is enabled.

Pump control definition: 0b = External V_{LCD} **1b = Internal V_{LCD} (x10)**

(7) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	0	0	1	1	0	0	0	R
(Double-byte command)	0	0	APC register parameter							

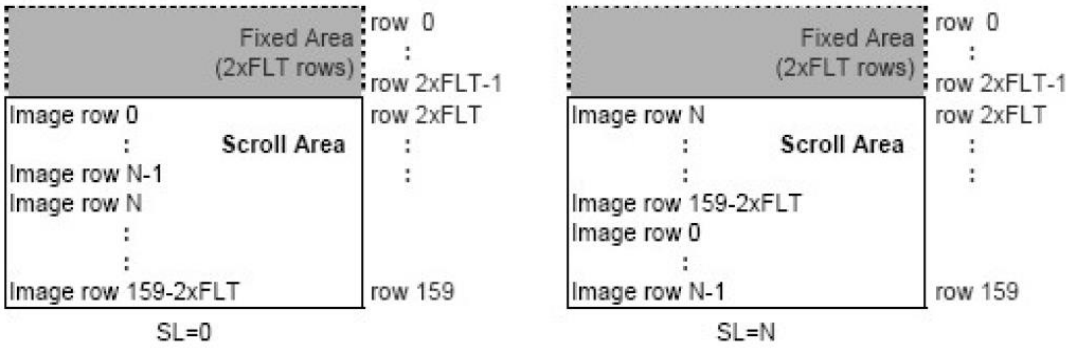
For UltraChip only. Please do NOT use.

(8) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	0	1	0	1	SL7	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the `Set Fixed Lines` command.



(9) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	0	1	1	0	RA3	RA2	RA1	RA0
Set Row Address MSB RA [7:4]	0	0	0	1	1	1	RA7	RA6	RA5	RA4

Set SRAM row address for read/write access.

Possible value = 0~159

(10) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	1	0	0	0	0	0	0	1
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section *LCD Voltage Setting* for more detail.

Effective range: 0 ~ 255

(11) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC[8]	0	0	1	0	0	0	0	1	0	LC8

This command is used to enable partial display function.

LC[8] : 0b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
1b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(12) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order
0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).
1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

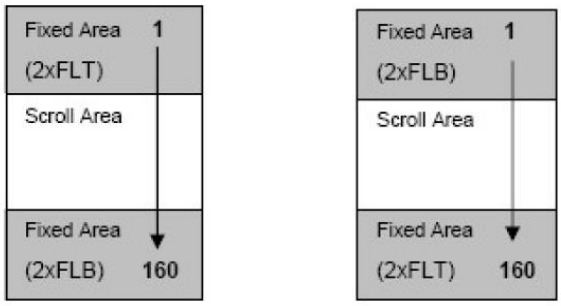
AC[2]: RID, row address (RA) auto increment direction (0/1 = +/- 1)
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program mode (AC[3]=ON), see section *Command Description* (32) ~ (35) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

(13) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB} (Double-byte command)	0	0	1	0	0	1	0	0	0	0
	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], ensure:

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(14) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 108, 80, 56, and 40.

The following are line rates at Mux Rate = 109 ~ 160.
00b: 25.2 Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps
In On/Off Mode
00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps
(Klps: Kilo-Line-per-second)

(15) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(16) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

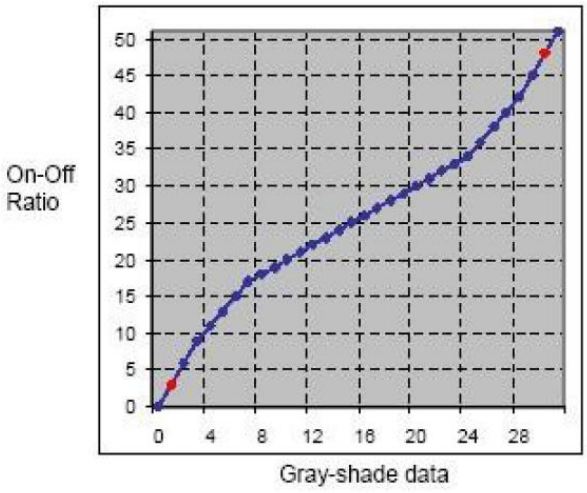
(17) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	1	0	1	0	1	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1698u will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1698u has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command `Set Color Mode` for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

1. For red and blue colors, when PWM is off, the shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. When PWM is on, these shades are produced by PWM.
2. Green shades are created by combining FRC (default: Off) and special dithering. When PWM is off, six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering while they are created by PWM when PWM is on. Data 62 and 63 are mapped to the same shade.
3. When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1698u for 5~10mS after setting DC[2] to 1.

(18) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

(19) SET N-LINE INVERSION

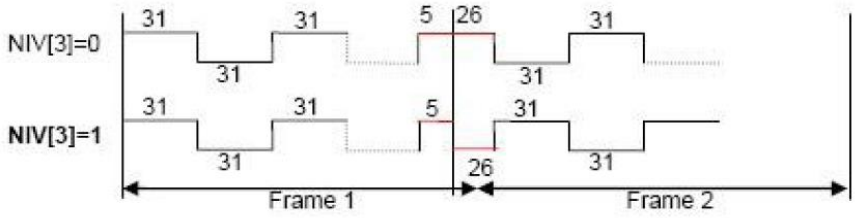
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line inversion NIV[3:0]	0	0	1	1	0	0	1	0	0	0
(Double-byte command)	0	0	-	-	-	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[2:0]: 000b: 11 lines; 001b: 19 lines; 010b: 21 lines; 011b: 25 lines; 100b: 29 lines; **101b: 31 lines**; 110b: 37 lines; 111b: 43 lines

NIV[3]: 0b: non-XOR; **1b: XOR**

NIV[4]: 0b: Disable NIV; **1b: Enable NIV**



(20) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	1	1	0	1	0	0	0	LC5

UC1698u supports on-chip swapping of R⇔B data mapping to the SEG drivers.

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG382	SEG383	SEG384
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in *Set Color Mode* below.

(21) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	1	1	0	1	0	1	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: *For serial bus modes, please refer to 8-bit tables below.*

Green Enhance Mode disabled (DC[4]=1):

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)

12 bits of input RGB data are stored to 16 RAM bits. No dither is performed. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	*D[7:0]*							
1st Write Data Cycle	R3	R2	R1	R0	G3	G2	G1	G0
2nd Write Data Cycle	B3	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G3	G2	G1	G0	B3	B2	B1	B0

Data Write Sequence (16-bit)	*D[15:0]*															
1st Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0
2nd Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = **10b** (RRRRR-GGGGGG-BBBBB, 64K-color)

16 bits of input data are stored to 16 RAM bits directly.

Data Write Sequence (8-bit)	*D[7:0]*							
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3
2nd Write Data Cycle	G2	G1	G0	B4	B3	B2	B1	B0

Data Write Sequence (16-bit)	*D[15:0]*															
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Green Enhance Mode enabled (DC[4]=0)**:**

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K-color)

12 bits of input data are extended and stored to 16 RAM bits. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	*D[7:0]*							
1st Write Data Cycle	R3	R2	R1	R0	G4	G3	G2	G1
2nd Write Data Cycle	G0	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G4	G3	G2	G1	G0	B2	B1	B0

Data Write Sequence (16-bit)	*D[15:0]*															
1st Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G4	G3	G2	G1	G0	B2	B1	B0
2nd Write Data Cycle	0	0	0	0	R3	R2	R1	R0	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

The behaviors of 8-bit input mode and 16-bit input mode do not change with DC[4] setting. Refer to previous section for more information on these two input modes.

(22) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	1	1	0	1	1	CSF2	CSF1	CSF0

COM scan function

CSF[0]: Interlace Scan Function
- **0b: LRM sequence: AEBCD-AEBCD**
- 1b: LRM sequence: AEBCD-EBCDA

CSF[1]: FRC Function
- **0b: FRC Disable**
- 1b: FRC Enable

CSF[2]: Shade-1, Shade-30 option
- **0 : Dither directly on input data(SRAM Change)**
- 1 : PWM on SEG output stage

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for "no operation".

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do *NOT* use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b =5 01b = 10 10b = 11 **11b = 12**

***(27)* SET COM END**

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	1	1	1	1	0	0	0	1
(Double-byte command)	0	0	-	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 160 pixel rows, the LCM designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes.

(28) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	1	1	1	1	0	0	1	0
(Double-byte command)	0	0	-	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(29) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	1	1	1	1	0	0	1	1
(Double-byte command)	0	0	-	*DEN* register parameter						

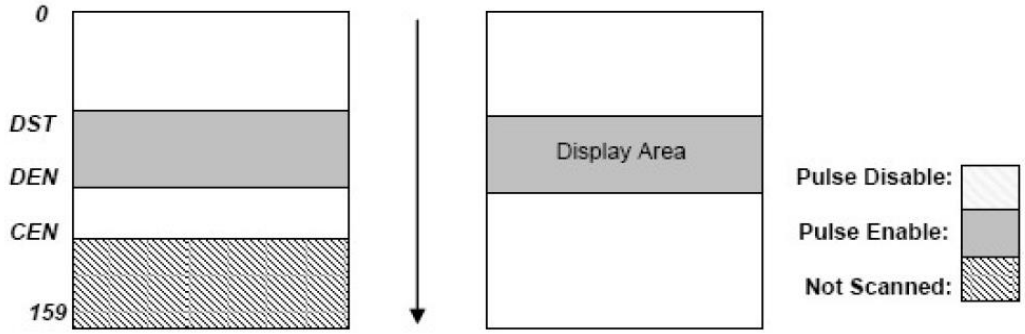
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1b, the Mux-Rate is narrowed down to DST-DEN+1+(FLT+FLB)xLC[0]x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[8]=1b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On/Off mode, set PC[0]=0b, disable N-Line Inversion, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 40, it is recommended to set BR=5 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(30) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (Double-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	-	*WPC0[6:0]* register parameter						

This command is to program the starting column address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (Double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	*WPP0[7:0]* register parameter							

This command is to program the starting row address of RAM program window.

(32) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	-	*WPC1[6:0]* register parameter						

This command is to program the ending column address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (Double-byte command)	0	0	1	1	1	1	0	1	1	1
	0	0	*WPP1[7:0]* register parameter							

This command is to program the ending row address of RAM program window.

(34) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	1	1	1	1	1	0	0	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under "Inside" mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay *within* the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

When Window Programming is under "Outside" mode, the CA and RA increment and wrap-around boundary will cover the entire UC1698u SRAM map (CA: 0~127, RA:0~159). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

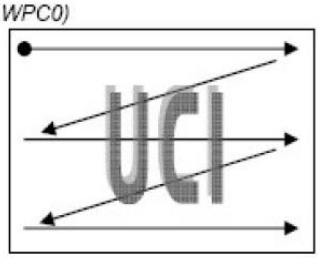
- WA (AC[0]) decides whether the program RAM address advances to next row / column after reaching the specified window column / row boundary.
- RID (AC[2]) controls the RAM address increasing from WPP0 toward WPP1 (RID=0) or the reverse direction (RID=1).
- Auto-increment Order (AC[1]) directs the RAM address increasing vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX (LC[1]) results the RAM column address increasing from 127-WPC0 to 127-WPC1 (MX=1) or from WPC0 to WPC1 (MX=0).

By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the "window", effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

Auto-increment order = 0 MX=0 RID = 0

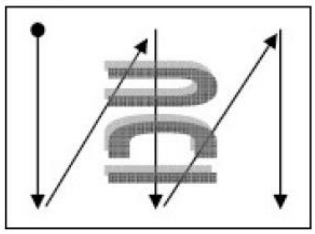
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 0

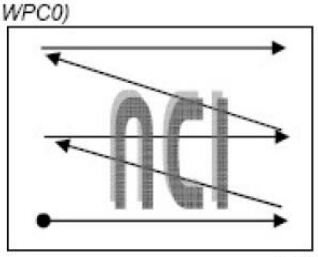
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=0 RID = 1

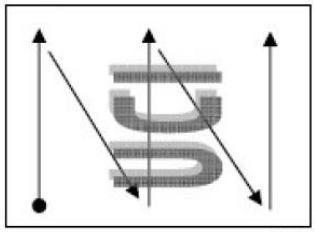
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 1 MX=0 RID = 1

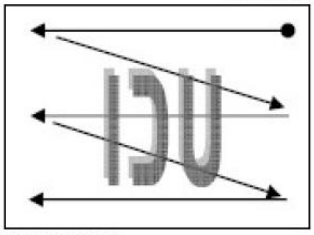
(WPP0,WPC0)



(WPP1,WPC1)

Auto-increment order = 0 MX=1 RID = 0

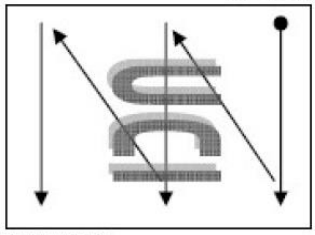
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 1 MX=1 RID = 0

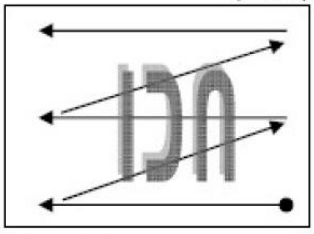
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 0 MX=1 RID = 1

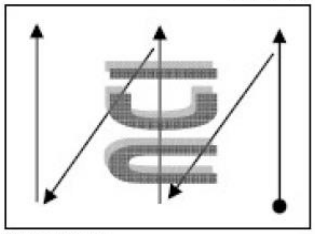
(WPP0,127-WPC0)



(WPP1,127-WPC1)

Auto-increment order = 1 MX=1 RID = 1

(WPP0,127-WPC0)



(WPP1,127-WPC1)

(35) SET MTP OPERATION CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (Double-byte command)	0	0	1	0	1	1	1	0	0	0
	0	0	-	-	-	*MTPC* register parameter				

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Sleep
001 : MTP Read
010 : MTP Erase
011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)
DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

The following commands, (37) ~ (41), are used as MTP commands only when MTPC[3]=1.

(36) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (Triple-byte command)	0	0	1	0	1	1	1	0	0	1
	0	0	-	MTPM[6:0] register parameter						
	0	0	-	-	-	-	-	-	MTPM1 [1:0]	

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no Write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[6:0] : Set PMO value
MTPM1[1:0]: Set MID value

This command is only valid when MTPC[3]=1.

(37) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (Double-byte command)	0	0	1	1	1	1	0	1	0	0
	0	0	Shared register parameter							

This command is for fine tuning V_{MPT1} setting (use with BR=00) and is only valid when MTPC[3]=1.

(38) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (Double-byte command)	0	0	1	1	1	1	0	1	0	1
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} PM setting (use with BR=01) and is only valid when MTPC[3]=1.

(39) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (Double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(40) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (Double-byte command)	0	0	1	1	1	1	0	1	1	1
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

LCD VOLTAGE SETTING

Multiplex Rates

Multiplex Rate is completely software programmable in UC1698u via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1698u can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

Bias Ratio Selection

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=160), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally can not maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as Mux Rate decreases, and the shades near the two ends of the spectrum will start to lose visibility.

UC1698u supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

Temperature Compensation

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per °C	-0.00	-0.05	-0.15	-0.25

Table 2: Temperature Compensation

V_{LCD} and Contrast Fine Tuning

Color STN LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the V_{OP} of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to precisely match the actual V_{OP} of each LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

Load Driving Strength for COG

The power supply circuit of UC1698u is designed to handle LCD panels with loading up to ~18nF using 7-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.8V$. For larger LCD panels, use lower resistance ITO glass.

Due to crosstalk consideration, ~18nF is also the recommended maximum LCD panel loading for COG applications. Using 4.5-Ω/Sq low resistance ITO glass will help improve image quality and operation tolerance.

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[1].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

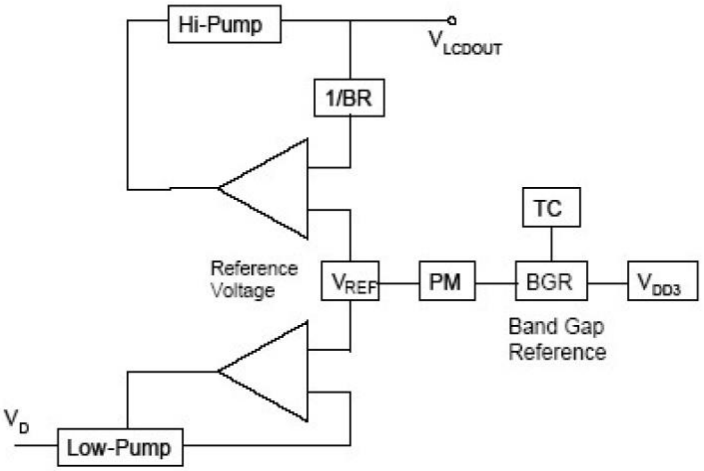
where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

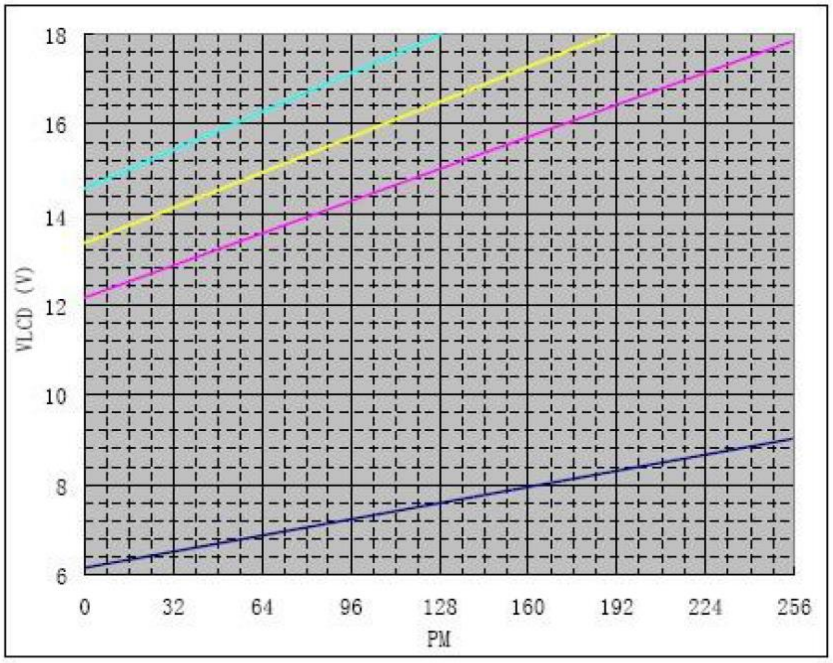
PM is the numerical value of PM register,

T is the ambient temperature in ^{o}C, and

C_T is the temperature compensation coefficient as selected by TC register.



V_{LCD} QUICK REFERENCE



BR	C_{V0} (V)	C_{PM} (mV)	PM_reg	V_{LCD} (V)
5	6.154	11.22	0	6.154
			255	9.015
10	12.157	22.26	0	12.157
			255	17.833
11	13.369	24.45	0	13.369
			189	17.991
12	14.580	26.61	0	14.580
			128	17.986

V_{LCD}-PM-BR relationship at 25°C

NOTE:

1. For good product reliability, please keep V_{LCD} under **18V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1698u contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 109, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate.

When Mux-Rate is lowered to 108, 80, 56 and 40, line rate will be scaled down automatically by 1.5, 2, 3 and 4 times to reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Line rate 37.0 Klps or higher is recommended for 32-shade mode. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When switching from 32-shade modulation to On/Off Mode, line rate will be scaled down automatically to reduce power.

Under most situations, flicker behavior is similar between these two modulation schemes. However, it is recommended to test each mode to make sure the result is as expected.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via the `Set Display Enable` command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1698u will put itself into Sleep mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1698u will first exit from Sleep mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Driver Modes

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG drivers are in Idle mode, they will be connected together to ensure zero DC condition on the LCD.

Driver Arrangements

The naming convention is COM(*X*), where *X* =1~160, referring to the COM driver for the *X*-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

Display Controls

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

Control register FLT and FLB specify two regions of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. FLT and FLB registers can be used to implement fixed regions when the other part of the display is scrolled by SL.

Partial Display

UC1698u provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

Gray-shade Modulation Mode

UC1698u has two gray-shade modulation modes: 32-shade and On/Off Mode.

The On/Off mode will consume roughly 40~45% less power than the 32-shade mode, and can be used for situations where power consumption is more critical than color fidelity.

Changing gray-shade modulation mode does not affect the content of SRAM display buffer, and the image data will remain the same after switching back and forth between On/Off mode and 32-shade mode.

Input Color Formats

UC1698u supports the following two different input color formats.

4KC (12-bit/RGB): In this color mode, R/G/B will be extended and the input data will be converted into 5R-6G-5B format before they are stored to display RAM.

64KC (16-bit/RGB): This is the native color mode. Data will be stored directly to on-chip SRAM in 5R-6G-5B (16-bit) format (except shade1 and shade30, which are achieved by special dithering. See command Set Display Enable for more details). This is the default input format mode.

Changing color mode does not affect the content already stored in the display buffer RAM. Users can mix several color modes together and switch among them in real time.

For example, the menu portion can be painted in 4K-color mode for fast update speed, and then switch to 64K-color mode, together with window programming function to effectively produce smooth graphics images.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data (depend on color mode) are stored to a dual port static RAM (RAM, for Display Data RAM) organized as 160x128X16.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and Set Column Address commands.

f wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the end of row 159), and system programmers need to set the values of RA and CA explicitly.

f WA is ON (1), when CA reaches the end of a row, CA will be reset to 0 and RA will increment or decrement, depending on the setting of row ncrement Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 159), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (127–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect on the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FTB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field

Line = *SL*

Otherwise

Line = Mod(*Line*+1, 160)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the "loop around" effect as it effectively resets *Line* to 0 when *Line+1* reaches 160. Effects such as scrolling can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field

Line = Mod(*SL* + *MUX-1*, 160)
where MUX = CEN + 1

Otherwise

Line = Mod(*Line-1*, 160)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM are not affected by MY.

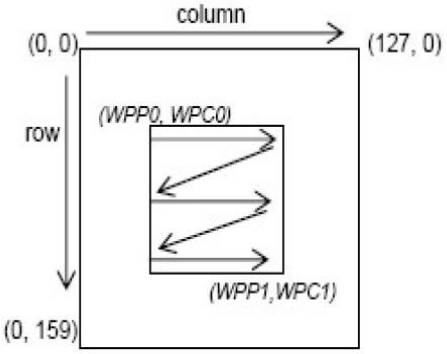
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and AC[3] setting for inside/outside window mode. When AC[3] is set to '0' (default value), data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). When AC[3] is set to '1', data will be written to whole SRAM excluding the specified window area.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either column or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial column address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

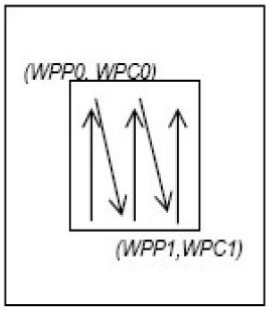
Example1 (AC[2:0] = 001) :

AC[3]=0 MX=0



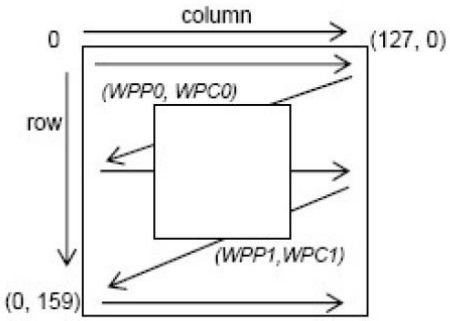
Example 2 (AC[2:0] = 111) :

AC[3] = 0 MX = 0



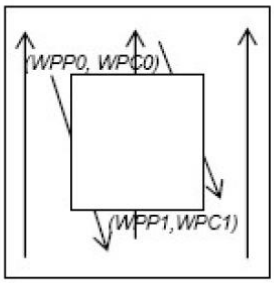
Example1-1 :

AC[3]=1 MX=0



Example 2-1 :

AC[3] = 1 MX = 0



Row Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H		COM1	COM17	COM160	COM16
01H		COM2	COM18	COM159	COM15
02H		COM3	COM19	COM158	COM14
03H		COM4	COM20	COM157	COM13
04H		COM5	COM21	COM156	COM12
05H		COM6	COM22	COM155	COM11
06H		COM7	COM23	COM154	COM10
07H		COM8	COM24	COM153	COM9
08H		COM9	COM25	COM152	COM8
09H		COM10	COM26	COM151	COM7
0AH		COM11	COM27	COM150	COM6
0BH		COM12	COM28	COM149	COM5
0CH		COM13	COM29	COM148	COM4
0DH		COM14	COM30	COM147	COM3
0EH		COM15	COM31	COM146	COM2
0FH		COM16	COM32	COM145	COM1
10H		COM17	COM33	COM144	COM160
11H		COM18	COM34	COM143	COM159
12H		COM19	COM35	COM142	COM158
13H		COM20	COM36	COM141	COM157
14H		COM21	COM37	COM140	COM156
15H		COM22	COM38	COM139	COM155
16H		COM23	COM39	COM138	COM154
17H		COM24	COM40	COM137	COM153
18H		COM25	COM41	COM136	COM152
19H		COM26	COM42	COM135	COM151
1AH		COM27	COM43	COM134	COM150
1BH		COM28	COM44	COM133	COM149
1CH		COM29	COM45	COM132	COM148
88H		COM137	COM153	COM24	COM40
89H		COM138	COM154	COM23	COM39
8AH		COM139	COM155	COM22	COM38
8BH		COM140	COM156	COM21	COM37
8CH		COM141	COM157	COM20	COM36
8DH		COM142	COM158	COM19	COM35
8EH		COM143	COM159	COM18	COM34
8FH		COM144	COM160	COM17	COM33
90H		COM145	COM1	COM16	COM32
91H		COM146	COM2	COM15	COM31
92H		COM147	COM3	COM14	COM30
93H		COM148	COM4	COM13	COM29
94H		COM149	COM5	COM12	COM28
95H		COM150	COM6	COM11	COM27
96H		COM151	COM7	COM10	COM26
97H		COM152	COM8	COM9	COM25
98H		COM153	COM9	COM8	COM24
99H		COM154	COM10	COM7	COM23
9AH		COM155	COM11	COM6	COM22
9BH		COM156	COM12	COM5	COM21
9CH		COM157	COM13	COM4	COM20
9DH		COM158	COM14	COM3	COM19
9EH		COM159	COM15	COM2	COM18
9FH		COM160	COM16	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
0												
1	SEG382	SEG383	SEG384	SEG379	SEG380			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st Byte write data: 11111111b

⇒ 2nd Byte write data: 11111111b

9. 产品使用说明

9-1.产品出厂说明

产品在我公司出厂前经过 100%的完全系统的检测，请在收到产品后确认包装是否完好，如有问题请直接和我公司联系，以确保后续的正常使用，减少不必要的麻烦；

9-2.产品说明

打开包装后请确认产品的型号是否正确，方便正常使用；

9-3 产品使用说明

9-3-1.静电防护

液晶显示模块中的液晶显示驱动芯片是大规模的 COMS 电路,极易被静电击穿,而静电击穿是不可修复,所以在操作、装配以及使用中都应严防静电,因此必须注意：

※ 不能用手随意接触液晶显示模块的驱动芯片与电路板上的金手指,若必须接触时，一定带上抗静电手环，防静电手指套/手套，最好穿上防静电工作服，使人体良好接地。

※ 工作台,烙铁及工具良好接地。

※ 工作间保持湿度在 RH60%以上。

9-3-2.焊接使用说明

※ 烙铁头温度小于 280±10℃。

※ 焊接时间小于 4S。

※ 不使用酸性助焊剂。

※ 重复焊接不超过 3 次,且每次重复需间隔 5 分钟以上。

※ 焊接后需要清洁,防止焊接短路和产生信号干扰,不能把药水渗透到产品内。

9-3-3.测试使用说明

※ 按接口定义连接产品各接口,注意正、负电源的极性不能搞错,否则造成过流、过压、烧毁电路上的芯片。

※ 正确接线后,开始测试液晶显示模块时,先打开逻辑电源,再打开液晶显示模块的驱动电源；断电时,先关掉液晶显示模块的驱动电源,再关掉逻辑电源。

※ 液晶显示模块的显示效果会随着温度的变化而相应变化。

9-4 产品存储说明

※ 建议装入聚乙稀口袋(最好有防静电涂层)并将口封住。

※ 在-10～+35℃之间存储。放暗处，避强光。不能在表面压放任何物品。

※ 严格避免在极限温 / 湿度条件下存放。特殊条件下必须存放时，也可在 40℃、85%RH 时，或 60℃，小于 60%RH 条件下存放，但不宜超过 168 小时。

※ 在运输途中不能剧烈震动或跌落，不能有外力压迫，并且无水、无尘也无日光直射。

10.附件一.驱动程序